UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,570	02/11/2004	Klaus J. Oberlaender	04303/0203690-US0	6012

38881 7590 09/08/2006

DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS 6TH AVENUE
NEW YORK, NY 10036-2714

EXAMINER	
THAI, TUAN V	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 09/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,570	OBERLAENDER ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 8-18 and 22* is/are rejected.

7)☒ Claim(s) *4-7 and 19-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. Claims 1-22 are presented for examination.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 8-18 and 22 are rejected under 35 U.S.C. § 102(e) as being anticipated by Janik et al. (USPN: 6,754,116); hereinafter Janik.

As per claim 1, Janik discloses the invention as claimed including a microprocessor system comprises an address generator

as being equivalent to the switching unit BIST configured to simultaneously generate a first memory address and a second memory address; for example, the BIST unit thereof for generating the command sequences so that commands that simultaneously address a plurality of memory banks are also generated (e.g. see column 2, lines 44-51; column 8, lines 5 et seq.); a memory system having a first memory tower/bank and a second memory tower/bank (e.g. see figures 2 and 3B, column 1, lines 64 et seq.); and an address selector coupled to receive the first memory address and the second memory address and configured to select a first row address for the first memory tower and a second row address for the second memory tower (e.g. see column 8, lines 40-56).

As per claim 2, Janik illustrates the first row address is equal to a row portion of the first memory address, and the second row address is equal to a row portion of the second memory address (e.g. see figure 3B);

As per claim 3, the further limitation of the first row address is equal to a row portion of the second memory address, and the second row address is equal to a row portion of the first memory address is taught by Janik since Janik discloses the row address are interchangeable for the same bank operation (e.g. see figure 3B; particularly for "Row Address" and "Bank Address RD, WR");

As per claims 8 and 9, Janik discloses the second memory address is one memory row greater than the first memory address or a row portion of the first memory address since Janik clearly teaches that first and second rows are processed in ***temporal succession*** (e.g. see column 8, lines 32 et seq.;);

As per claim 10; Janik discloses the second memory address is equal to a row portion of the first memory address plus 1 since the first and second row address commands are presented one below the other (e.g. see column 8, lines 35 et seq.);

As per claim 11, Janik discloses the data aligner as being equivalent to the BIST 2 coupled to the memory system (e.g. see figure 2);

As per claim 12, Janik discloses his memory system comprises multiple memory banks which are known to include third and fourth towers/banks as being claimed (e.g. see column 7, lines 15 et seq.);

As per claim 13, the further limitation of the address selector (MUX, figure 2) configured to select a third row address for the third memory tower and a fourth row address for the fourth memory tower is embedded in the system of Janik, since Janik discloses multiple towers/banks being addresses wherein different row addresses (up to 9 command sequence of columns 1 to 10) can be activated (e.g. see column 8, lines 48-56);

As per claim 14, Janik discloses the address selector (MUX)

is controlled by inputs address line 7 which is utilized for transmit addresses (the first memory address as being claimed) to the memory (e.g. see figure 2);

As per claim 15, Janik discloses the first row address is equal to a row portion of the first memory address (see figure 3B).;

As per claim 16, Janik discloses the second row address is equal to a row portion of the second memory address (e.g. figure 3B).

As per claim 17, it encompasses the same scope of invention as to that of claim 1 except that it is drafted as method format rather than the apparatus format, the claim is therefore rejected for the same reasons as being set forth above.

As per claim 18, Janik discloses performing a memory access using both the first row address and the second row address (e.g. see column 2, lines 44 et seq.; column 8, lines 40 et seq.);

As per claim 22, Janik discloses that the row portion of the second memory address is the same as the second memory address.

Allowable subject matter

5. Claims 4, 19 and 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. The prior arts of records do not

teach nor disclose the address generator further comprises a first adder and a second adder for generating first and second memory addresses respectively; in addition, the prior arts of record do not further teach adding a first memory operand and a second memory operand to generate the first memory address; adding the first operand, the second operand and a carry bit to generate the second memory address (claim 19), and adding the first memory operand and a second memory operand to generate the first memory address, adding a row portion of the first memory operand, a row portion of the second memory operand, and a carry bit to generate the second memory address (claim 21). Claims 5-7 and 20 are also objected to since they depended upon the indicated-objectable claim 4 respectively.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/September 03, 2006

Tuan V. Thai
PRIMARY EXAMINER
Group 2100